What is claimed is:

1. A system comprising:

a bus;

an external memory coupled to the bus;

a processor coupled to the memory via the bus, the processor to receive a plurality of instructions from the memory, wherein the processor is to:

advance an instruction in an instruction sequence predicted not to be executed through an instruction pipeline,

store in a mispredicted path side memory in parallel a result of the instruction in the instruction sequence that is predicted not to be executed from the instruction pipeline, and

restore in parallel the result from the store into the instruction pipeline for continued execution if an instruction in an instruction sequence predicted to be executed is mispredicted.

2. The system of claim 2, wherein the processor is to further:

advance the instruction in the instruction sequence predicted to be executed through the instruction pipeline.

3. The system of claim 2, wherein the processor is to further:

discard the stored result of the instruction that is predicted not to be executed if the instruction in the instruction sequence predicted to be executed was predicted correctly.

4. The system of claim 2, wherein the processor is to further:

predict that another instruction will be executed;

advance the another instruction through the instruction pipeline;

determine if the another instruction was predicted correctly; and

restore in parallel the result from the store into the instruction pipeline for continued execution if the another instruction was not predicted correctly.

5. The system of claim 2, wherein the mispredicted path side memory is a cache memory located internal to the processor.

6. A method for branch misprediction recovery in a multi-stage pipelined processor, the method comprising:

advancing an instruction in an instruction sequence predicted not to be executed through a plurality of instruction pipeline stages;

storing in a mispredicted path side memory, each stage in parallel, a result of the instruction in the instruction sequence that is predicted not to be executed from the plurality of instruction pipeline stages; and

restoring in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution if an instruction in an instruction sequence predicted to be executed is mispredicted.

7. The method of claim 6, further comprises:

predicting at a branch, the instruction sequence predicted to be executed and the instruction sequence predicted not to be executed.

8. The method of claim 6, further comprises:

if the instruction in the instruction sequence predicted to be executed was predicted correctly, discarding the stored result of the instruction that is predicted not to be executed.

9. The method of claim 6, further comprising:

predicting that another instruction will be executed;

advancing the another instruction through the plurality of stages;

determining if the another instruction was predicted correctly; and

if the another instruction was not predicted correctly, restoring in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution.

10. Apparatus for branch misprediction recovery, comprising:

a plurality of instruction pipeline stages to advance an instruction in an instruction sequence predicted not to be executed;

a mispredicted path side memory to store in parallel a result of the instruction in the instruction sequence that is predicted not to be executed from the plurality of instruction pipeline stages; and

a branch execution unit to determine if an instruction in an instruction sequence predicted to be executed is mispredicted and if an instruction in an instruction sequence predicted to be executed is mispredicted, the branch execution unit to restore in parallel the result from the mispredicted path side memory into the plurality of instruction pipeline stages for continued execution.

11. The apparatus of claim 10, further comprising:

a branch prediction unit to predict, at a branch, that an instruction sequence will be executed and an instruction sequence will not to be executed.

12. The apparatus of claim 10, further comprising:

a mispredicted memory control unit to transmit a read mispredicted path side memory signal to the mispredicted path side memory and in response, the mispredicted path side memory is to restore the result into the plurality of instruction pipeline stages in parallel.

13. The apparatus of claim 12, further comprises:

a mispredicted data line that is to couple each stage of the plurality of instruction pipeline stages to the mispredicted path side memory and to transfer a result from that stage to the mispredicted path side memory.

14. The apparatus of claim 13, further comprises:

a recovery branch data line that is to couple each stage of the plurality of instruction pipeline stages to the mispredicted path side memory and to restore a result from the mispredicted path side memory to that stage.

15. The apparatus of claim 13, further comprises:

a multiplexer that is coupled at a first input to a stage of the plurality of pipeline stages via an input data line and is coupled at a second input to the mispredicted path side memory via the recovery path side data line.

16. The apparatus of claim 15, wherein the multiplexer is coupled at an output to a next stage via an output data line and is coupled at the output to the mispredicted path side side memory via the mispredicted data line.

17. A system for branch misprediction recovery, the system comprising:

a bus;

an external memory coupled to the bus;

a processor coupled to the memory via the bus, the processor to receive a plurality of instructions from the memory, wherein the processor is to:

predict at a branch, an instruction sequence predicted to be executed and an instruction sequence predicted not to be executed;

advance an instruction in the instruction sequence that is predicted not to be executed through a plurality of instruction pipeline stages for execution;

store to a mispredicted path side memory, each stage in parallel, a result of the instruction in the instruction sequence that is predicted not to be executed from the plurality of instruction pipeline stages;

advance an instruction in the instruction sequence predicted to be executed through the plurality of instruction pipeline stages for execution after the instruction in the instruction

sequence that is predicted not to be executed is advanced;

determine if the instruction in the instruction sequence predicted to be executed was predicted correctly; and

restore in parallel the result from the storing operation into the plurality of instruction pipeline stages for continued execution if the instruction in the instruction sequence predicted to be executed was mispredicted.

18. The method of claim 17, wherein the processor is to further

discard the stored result of the instruction that is predicted not to be executed if the instruction in the instruction sequence predicted to be executed was predicted correctly.

19. The system of claim 17, wherein the processor is to further:

predict that another instruction will be executed;

advance the another instruction through the instruction pipeline;

determine if the another instruction was predicted correctly; and

restore in parallel the result from the store into the plurality of instruction pipeline stages for continued execution if the another instruction was not predicted correctly.

20. The system of claim 17, wherein the mispredicted path side memory is a cache memory located internal to the processor.